# Chapter 1. PCI Express

# （Peripheral Component Interconnect Express）

## 1.1 Product Overview

The Sirius PCIe provides an AXI4 bridging capability for directly adding the PCI Express link to Network on Chip through AXI system fabric. The bridge interconnects the AXI interfaces within an AXI-embedded system with a remote PCIe link, as either a root complex port or as an endpoint port. The bridge supports three AXI interfaces:

■ one masters

■ one link slave

■ one DBI slave

The AXI master interfaces enable a remote PCIe device to read and write to an AXI slave connected to the NOC, like DDR slave. The AXI link slave interface enables an AXI master, Top DMAC for example, to read and write through the NOC to a remote PCIe device. The DBI slave enables an AXI master, A7 core for example, to access the PCIe’s registers. The Sirius PCIe supports up to x2 Gen1/Gen2 lanes, and the max throughput is 10 Gb/s.

## 1.2 Architecture

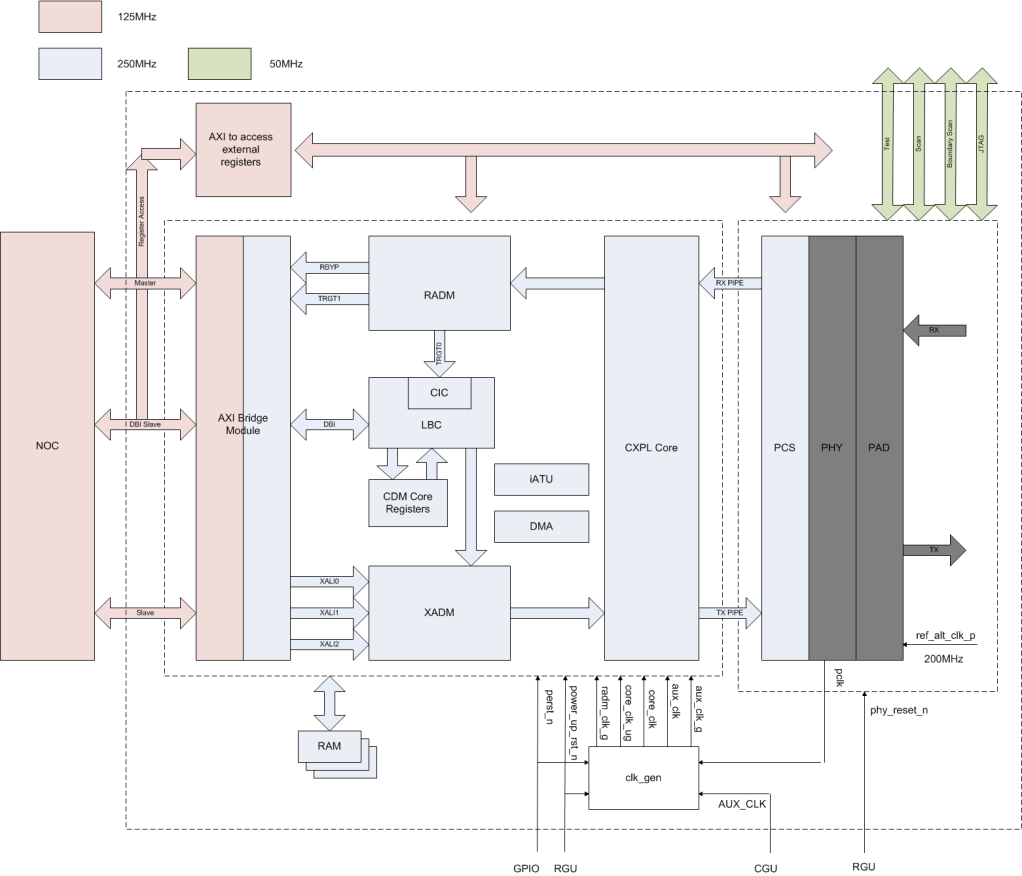


Figure 1.1 PCIe Architecture

PCIe module includes two parts: PCIe DM controller and PCIe PHY, as shown in Figure 1.1. The physical layer is split across the PIPE and controller such that the MAC functionality (LTSSM, lane-to-lane deskew) is in the controller and the PHY functionality is implemented in the PIPE-compliant PHY. The PHY is outside of the controller, interfacing through the standard PIPE interface.

### 1.2.1 PCIe DM controller

This PCIe dual mode (DM) controller provides a solution to implement a PCI Express port for a PCI Express root complex or endpoint application. The operating mode of the controller (root complex or endpoint) is determined by the device\_type input pin at power-up.

The implementation of the PCIe protocol and mode-specific features is split across several modules.

■ **Common Express Port Logic (CXPL) Module:** implements the basic functionality for the PCI Express physical, link, and transaction layers.

■ **Transmit Application-Dependent Module (XADM):** implements application-specific functionality of the PCI Express transaction layer for packet transmission.

■ **Receive Application-Dependent Module (RADM):** implements application-specific functionality of the PCI Express transaction layer for packet reception.

■ **Configuration-Dependent Module (CDM):** implements Standard PCI Express configuration space and Controller-specific register space (Port Logic Registers).

■ **Power Management Controller (PMC):** implements the power management features of the controller.

■ **Local Bus Controller (LBC) and Data Bus Interface (DBI):** provides a mechanism for a link partner (in EP mode only) or a local CPU (through the DBI) to access Internal registers (in the CDM) and External application registers connected externally to the ELBI.

■ **Message Generation Module (MSG\_GEN):** transmits messages generated by the controller.

■ **Hot Plug Control Module (HOTPLUG):** implements logic to generate interrupts on hot plug events.

■ **Embedded Multichannel DMA Controller (DMA):** offload the transferring of large blocks of data to the embedded DMA controller, leaving the CPU free to perform other tasks.

### 1.2.2 PCIe PHY

This PCIe PHY implements complete PCI Express 2.0 physical layer capability for 5-Gbps operation, connecting a root complex, switch, or endpoint to a PCI Express system. This PCIe PHY supports the 5-Gbps data rate of the PCI Express Gen 2 specification and is backward compatible with the 2.5-Gbps Gen 1.1 specification with only inferred idle detection supported. It is targeted for the second generation connectivity in chip-to-chip or card-to-card communication across a combination of printed circuit board, connectors, backplane wiring, or cable.

## 1.3 Features

* The Sirius PCI Express supports：  
  ■ All non-optional features of the *PCI Express 2.0*  
  ■ x2 Gen1, Gen2 lanes  
  ■ 32-bit Internal Datapath Operating at 125 or 250 MHz  
  ■ Advanced Power and Clock Management

■ Internal Address Translation Unit  
 ■ Internal MSI-X Generation Module

■ AXI4 bridge

■ Two Embedded DMA

■ Automatic Lane Reversal

■ Upconfigure Support

■ Bypass, Cut-through, and Store-and-forward Queue Modes for Rx TLPs

■ Three Application Transmit Clients

■ Type 0 / 1 Configuration space

■ PHY Control Registers access

■ 5-Gbps data transmission rate

■ Integrated PHY includes transmitter, receiver, PLL, digital core, and electrostatic discharge (ESD) protection circuits

■ Excellent performance margin and receiver sensitivity

■ Robust PHY architecture that tolerates wide process, voltage, and temperature variations

■ Low-jitter PLL technology with excellent supply isolation

■ Built-in Self-Test (BIST) features for production, at-speed testing on any digital tester

■ Visibility and controllability of hard macro functions through programmable registers in the design